Remarks

I. Introduction

Claims 14 to 24 are pending in the present application. Claims 14, 19 and 20 have been amended. In view of the preceding amendments and the following remarks, it is respectfully submitted that all of the presently pending claims are allowable, and reconsideration is respectfully requested.

II. Rejection of Claims 19 and 20 Under 35 U.S.C. § 112, Second Paragraph

Claims 19 and 20 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. In response, claims 19 and 20 have been amended to clarify the subject matter therein. It is, therefore, respectfully submitted that claims 19 and 20 are not indefinite, and it is respectfully requested that this rejection be withdrawn.

III. Rejection of Claims 14 to 24 Under 35 U.S.C. § 103(a)

Claims 14 to 24 stand rejected under 35 U.S.C. § 103(a) ad being unpatentable over the combination of U.S. Patent No. 5,738,757 ("Burns et al.") and U.S. Patent No. 6,033,997 ("Perng"). It is respectfully submitted that the combination of Burns et al. and Perng does not render obvious claims 14 to 24 for the following reasons.

Amended claim 14 recites a method including providing a wafer having a surface and edge areas, dividing the surface of the wafer into positive areas and negative areas, the negative areas including the edge areas of the wafer, providing the negative areas with a first passivation layer to protect the negative areas from a subsequent second etching process, providing at least one of the positive areas with a second passivation layer having a thickness that is less than a thickness of the first passivation layer, selectively removing the second passivation layer via a first etching process, the first etching process being terminated when the second passivation layer is completely removed, subsequently etching the wafer via the second etching process, and removing the first passivation layer. Claims 15 to 24 ultimately depend from claim 14.

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970). In order for a claim to be rejected for obviousness under

35 U.S.C. § 103(a), not only must the prior art teach or suggest each element of the claim, the prior art must also suggest combining the elements in the manner contemplated by the claim. See Northern Telecom, Inc. v. Datapoint Corp., 908 F. 2d 931, 934 (Fed. Cir. 1990); In re Bond, 910 F. 2d 831, 834 (Fed. Cir. 1990). The Examiner bears the burden of showing: 1) some suggestion or motivation to modify or combine the reference teachings in the prior art, and not based on the applicant's disclosure; 2) a reasonable expectation of success; and 3) the combined references teach or suggest all the claim limitations. See M.P.E.P. §2143; see also In re Vaeck, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Applicants respectfully submit that the Examiner has failed to satisfy this burden.

Burns et al. purport to relate to planar masking for multi-depth silicon etching. The Office Action asserts that the Burns et al. reference, "discloses a method comprising...dividing the surface of the wafer into positive areas (unmasked and partially masked areas in the figures)...and negative areas (masked areas) including the edge areas of the wafer (since the figures show that the edges are not etched)." See page 2 of the Office Action.

Initially, it is noted that the Examiner's definition of positive and negative areas is not consistent with that provided by the Applicants' specification, for example, page 3, lines 1-14. Furthermore, it is submitted that the Burns et al. reference does not disclose, or even suggest, that the unmasked and partially masked areas are equivalent to the positive areas, or that the masked areas are negative areas, as asserted in the Office Action. Burns et al. does not disclose, or even suggest, dividing the surface of the wafer into positive areas and negative areas, at all. Burns et al. actually recites that, "the process involves the application of several alternating masking layers (e.g. of silicon dioxide and silicon nitride) on a planar silicon wafer." Col. 4, line 66 to col. 5, line 2. The Office Action reflects an unsubstantiated assumption that the edges of the planar silicon wafer 10 are not etched and therefore must be masked. However, Burns et al. does not disclose, or even suggest, that the edges are not etched or that they are masked. As stated above, each of figures 1A through 1I depicts a left edge of the planar silicon wafer 10, and shows that the edge is exposed and not masked. Furthermore, the Office Action later admits that, "Burns [et al.] does not disclose providing the edge areas with a passivation layer." Office Action at page 3.

Furthermore, the unmasked edge areas of Burns et al. would, by the characterization provided in the Office Action, be positive areas. Therefore, Burns et al. does not disclose, or even suggest, dividing the surface of the wafer into positive areas and negative areas, the negative areas including the edge areas of the wafer, as recited in claim 14.

Furthermore, the Office Action asserts that the Burns reference "discloses...providing the negative areas with a first passivation layer (the combination of layers 12, 14, 16, and 18)...[and] providing at least one of the positive areas with a second passivation layer (the combination of layers 12 and 14 in Figure 1B)." See page 3 of the Office Action. Although Applicants disagree with this characterization, it is noted that even if layers 12, 14, 16, and 18 were equated with a first passivation layer, and layers 12 and 14 were equated with a second passivation layer, this characterization is contrary to claim 14. Amended claim 14 recites "removing the second passivation layer via a first etching process, the first etching process being terminated when the second passivation layer is completely removed, subsequently etching the wafer via the second etching process, and removing the first passivation layer." According to the Office Action, the first etching process would purportedly remove layers 12 and 14 (the second passivation layer), and would be terminated when layers 12 and 14 are completely removed. Subsequently, during the second etching process, layers 12, 14, 16, and 18 (the first passivation layer) would be removed. Since layers 12 and 14 cannot be completely removed without completely removing layers 16 and 18 first, the Burns et al. reference does not disclose, or even suggest, removing the second passivation layer via a first etching process, the first etching process being terminated when the second passivation layer is completely removed, subsequently etching the wafer via the second etching process, and removing the first passivation layer, as recited in claim 14.

The Office Action asserts in the Response to Arguments section, that the claims "are not limited to any particular order of the etching steps." While this may be generally true where no indication of the order of the steps is provided, amended claim 14 recites "a first passivation layer to protect the negative areas from a subsequent second etching process." Claim 14 has been amended to further recite "selectively removing the second passivation layer via a first etching process, the first etching process being terminated when the second passivation layer is completely removed [and] subsequently etching the wafer via the second etching process." (Emphasis added.) Therefore, the second etching process recited in claim 14 occurs subsequent to the first etching process.

In summary, Burns et al. do not disclose, or even suggest, dividing the surface of the wafer into positive areas and negative areas, the negative areas including the edge areas of the wafer, as recited in claim 14. Furthermore, Burns et al. do not disclose, or even suggest, providing the negative areas with a first passivation layer to protect the negative areas from a subsequent second etching process, providing at least one of the positive areas with a second

passivation layer having a thickness that is less than a thickness of the first passivation layer, selectively removing the second passivation layer via a first etching process, the first etching process being terminated when the second passivation layer is completely removed, subsequently etching the wafer via the second etching process, and removing the first passivation layer, as recited in claim 14. Therefore, it is respectfully submitted that Burns et al. does not render claim 14 obvious.

The secondary reference, Perng, does not cure the deficiencies of Burns et al., i.e., Perng does not disclose, or even suggest, dividing the surface of the wafer into positive areas and negative areas, the negative areas including the edge areas of the wafer, as recited in claim 14. Furthermore, Perng does not disclose, or even suggest, providing the negative areas with a first passivation layer to protect the negative areas from a subsequent second etching process, providing at least one of the positive areas with a second passivation layer having a thickness that is less than a thickness of the first passivation layer, selectively removing the second passivation layer via a first etching process, the first etching process being terminated when the second passivation layer is completely removed, subsequently etching the wafer via the second etching process, and removing the first passivation layer, as recited in claim 14. Therefore, it is respectfully submitted that Perng does not render claim 14 obvious.

It is therefore respectfully submitted that for at least the above reasons, the combination of Burns et al. and Perng does not render obvious claim 14. As for claim 15 to 24, which depend from claim 14 and include all of the features of claim 14, it is respectfully submitted that the combination of Burns et al. and Perng does not render obvious claim 15 to 24 for at least the same reasons given above in support of the patentability of claim 14.

Furthermore, with respect to claim 15, the Office Action asserts that "the nitride layer 18 defines a part of the surface of the wafer." Office Action page 3. As the Office Action previously defined nitride layer 18 as a sublayer of the masking layer of Burns et al. in the rejection of claim 14, this new definition is contrary to the definition previously espoused in the Office Action. In any case, Applicants respectfully traverse this contention, and further submit that both definitions cannot be simultaneously adopted.

With respect to claim 16, the Office Action asserts that Burns "discloses to remove the nitride layer in subareas (where 18 is not present in Figure 1B) after the passivation layer is provided." However, even if layer 18 is removed according to the Office Action's characterization of the purported first passivation layer of Burns et al., a layer of silicon nitride 14 below layer 18 still remains, and therefore, the nitride layer has not been removed.

Therefore, Burns et al. do not disclose or even suggest "the step of removing the nitride layer at least in subareas of the positive areas after the negative areas are provided with the first passivation layer and before the wafer is etched," as recited in claim 16.

With respect to claim 17 and 18, the Office Action asserts that "it would have been obvious to remove photoresist after exposing and developing because it is not useful during subsequent processing of the substrate." Applicants respectfully traverse this unsubstantiated assumption, and note that, as provided in the Specification, according to standard IC photoresist technique, the resist may be removed from the edges before exposure. See Specification, page 4, lines 12 to 16.

With respect to claim 19, "Examiner takes official notice that it is conventional in the art to form oxide layers by a LOCOS process. It would have been obvious to one with ordinary skill in the art to use a LOCOS process to form the oxide layer in the method of Burns because it is a conventional technique for forming oxide layers." Applicants respectfully traverse this unsupported assertion. According to Burns et al., entire planar layers are provided of silicon dioxide and silicon nitride, one over another. LOCOS, or local oxidation of silicon, however, provides for a layer of oxide to be grown on a silicon substrate in only those areas where have not been layered with nitride. Therefore, the figures of Burns et al., as well as the above characterization upon which the Office Action relies, require that entire planar layers of oxide are provided over entire planar layers of nitride, an arrangement for which it may not be practical to use a LOCOS process. Therefore, it is respectfully submitted that claim 19, which recites, applying the oxide layer in a LOCOS process, is not rendered obvious by Burns et al. in view of the prior art. In any case, the Examiner is requested to provide a documentary support for the official notice, which is a conclusion based on Examiner's personal knowledge. M.P.E.P. § 2144.03.

With respect to claim 20, the Office Action asserts that, "Burns [et al.] discloses that the first and second passivation layers comprise oxide." Applicants respectfully traverse this unsupported assumption, as Burns et al. does not disclose, or even suggest, a first or a second passivation layer comprising an oxide.

In summary, it is respectfully submitted that the combination of Burns et al. and Perng does not render claims 14 to 24 obvious for at least the above reasons, and it is respectfully requested that the rejection of claims 14 to 24 under 35 U.S.C. § 103(a) be withdrawn.

IV. Rejection of Claims 14 to 24 Under 35 U.S.C. § 103(a)

Claims 14 to 24 stand rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,711,891 ("Pearce"). It is respectfully submitted that claims 14 to 24 are patentable over Pearce for the following reasons.

Claim 14 recites a method including providing a wafer having a surface and edge areas, dividing the surface of the wafer into positive areas and negative areas, the negative areas including the edge areas of the wafer, providing the negative areas with a first passivation layer to protect the negative areas from a subsequent second etching process, providing at least one of the positive areas with a second passivation layer having a thickness that is less than a thickness of the first passivation layer, selectively removing the second passivation layer via a first etching process, the first etching process being terminated when the second passivation layer is completely removed, subsequently etching the wafer via the second etching process, and removing the first passivation layer. Claim 15 to 24 all ultimately depend from claim 14.

Pearce purports to relate to wafer processing using a thermal nitride etch mask. In support of this rejection, the Office Action asserts that "Pearce discloses a method comprising...dividing the surface of the wafer into positive areas (unmasked and partially masked areas in the figures)...and negative areas (masked areas) including the edge areas of the wafer (since the figures show that the edges are not etched; note that edge is not clearly defined and encompasses the edge of the figure depicted in Figure 2)." See page 4 of the Office Action.

Initially, it is noted that the Examiner's definition of positive and negative areas is not consistent with that provided by the Applicants' specification, for example, page 3, lines 1-14. Furthermore, the Pearce reference does not disclose, or even suggest, that unmasked and partially masked areas are equivalent to the positive areas, or that masked areas are equivalent to the negative areas, as asserted in the Office Action. Pearce does not disclose, or even suggest, dividing the surface of the wafer into positive areas and negative areas, at all. Pearce actually recites that "[i]n Fig. 2, reference numeral 111 denotes a substrate which may be silicon...Reference numeral 131 denotes a patterned oxide...[and] [r]eference numeral 132 denotes a blanket layer of silicon nitride." Col. 1, lines 41 to 48. Therefore, according to Pearce, the edges of the silicon substrate 111 are unmasked areas. The edge area included in the Figures appears to be exposed, and only the upper surface appears to be covered by the patterned oxide 131 and the blanket layer of nitride 132. For example, Figures 1 to 3 and 5 to

9 depict at least one edge of the silicon substrate 111, and shows that the edge is exposed and not masked. Therefore, Pearce does not disclose, or even suggest, that the edges are not etched or that they are masked.

Furthermore, the unmasked edge areas of Pearce would, by the characterization provided in the Office Action, be positive areas. Therefore, Pearce does not disclose, or even suggest, dividing the surface of the wafer into positive areas and negative areas, the negative areas including the edge areas of the wafer, as recited in claim 14.

Additionally, regardless of how positive and negative areas are defined, the layer 132, which, according to the Office Action, is the second passivation layer, is simply a blanket layer deposited over the entire surface. Therefore, Pearce does not disclose, or even suggest, providing at least one of the positive areas with a second passivation layer, as recited in claim 14. Accordingly, Pearce does not disclose, or even suggest, a method including providing a wafer having a surface and edge areas, dividing the surface of the wafer into positive areas and negative areas, the negative areas including the edge areas of the wafer, providing the negative areas with a first passivation layer to protect the negative areas from a subsequent second etching process, providing at least one of the positive areas with a second passivation layer having a thickness that is less than a thickness of the first passivation layer, selectively removing the second passivation layer via a first etching process, the first etching process being terminated when the second passivation layer is completely removed, subsequently etching the wafer via the second etching process, and removing the first passivation layer, as recited in claim 14.

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970). In order for a claim to be rejected for obviousness under 35 U.S.C. § 103(a), not only must the prior art teach or suggest each element of the claim, the prior art must also suggest combining the elements in the manner contemplated by the claim. See Northern Telecom, Inc. v. Datapoint Corp., 908 F. 2d 931, 934 (Fed. Cir. 1990); In re Bond, 910 F. 2d 831, 834 (Fed. Cir. 1990). The Examiner bears the burden of showing: 1) some suggestion or motivation to modify or combine the reference teachings in the prior art, and not based on the applicant's disclosure; 2) a reasonable expectation of success; and 3) the combined references teach or suggest all the claim limitations. See M.P.E.P. §2143; see also

In re Vaeck, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Applicants respectfully submit that the Examiner has failed to satisfy this burden.

In summary, it is respectfully submitted that Pearce does not render claim 14 obvious for at least the above reasons. It is further submitted that Pearce does not render obvious claims 15 to 24, which ultimately depend from claim 14, for at least the reasons given above in support of the patentability of claim 14.

V. Conclusion

Applicants respectfully submit that the subject matter of the present application is new, non-obvious, and useful. Prompt consideration and allowance of the application are respectfully requested.

It is therefore respectfully submitted that all of the presently pending claims are allowable. All issues raised by the Examiner having been addressed, an early and favorable action on the merits is earnestly solicited.

Respectfully submitted,

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